Amendments to the Claims:

1. (Original) A wireless communication system, comprising:

transmitter circuitry comprising encoder circuitry for transmitting a plurality of frames;

wherein each of the plurality of frames comprises a primary synchronization code and a secondary synchronization code; and

wherein the encoder circuitry comprises:

circuitry for providing the primary synchronization code in response to a first sequence; and

circuitry for providing the secondary synchronization code in response to a second sequence and a third sequence;

wherein the second sequence is selected from a plurality of sequences, wherein each of the plurality of sequences is orthogonal with respect to all other sequences in the plurality of sequences; and

wherein the third sequence comprises a subset of bits from the first sequence.

2. (Original) The system of claim 1 wherein the first sequence comprises a hierarchical sequence.

3. (Original) The system of claim 1 wherein the first sequence comprises a Golay sequence.

4. (Original) The system of claim 1:

wherein the second sequence comprises a plurality of code words; and

wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

5. (Original) The system of claim 4 wherein the second sequence consists of fifteen of the code words.

6. (Original) The system of claim 5 wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences.

7. (Original) The system of claim 6:

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise sixteen Hadamard sequences selected as every sixteenth sequence in the defined order.

8. (Original) The system of claim 4 wherein the second sequence consists of sixteen of the code words.

9. (Original) The system of claim 8 wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences.

10. (Original) The system of claim 6:

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise seventeen Hadamard sequences selected as every eighth sequence in the defined order.

11. (Original) The system of claim 1 wherein the circuitry for providing the secondary synchronization code comprises:

circuitry for performing an exclusive OR operation between the second sequence and the third sequence; and

circuitry for providing the secondary synchronization code in response to the exclusive OR operation.

12. (Original) The system of claim 1:

wherein the primary synchronization code comprises 8-bit values A and B and complements of the values A and B;

wherein the value A comprises a sequence A = { 1, 1, 1, 1, 1, 1, -1, -1 };

wherein the value B comprises a sequence B = { 1, -1, 1, -1, 1, -1, -1, 1 }; and

wherein the primary synchronization code comprises a 256-bit sequence {A, B, A, B, A, B, -A, -B, -A, -B, A, B, -A, -B, -A, -B, A, B, A, B, A, B, -A, -B, A, B, -A, -B, A, B, A, B}.

13. (Original) The system of claim 12:

wherein the second sequence comprises 256 bits; and

wherein the third sequence comprises 32 repeated instances of the value A.

14. (Original) The system of claim 13 wherein the circuitry for providing the secondary synchronization code comprises:

circuitry for performing an exclusive OR operation between the second sequence and the third sequence; and

circuitry for providing the secondary synchronization code in response to the exclusive OR operation.

15. (Original) The system of claim 14:

wherein the second sequence comprises a plurality of code words; and

wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

16. (Original) The system of claim 12:

wherein the second sequence comprises 256 bits;

wherein a complement of the value A is represented as –A; and

wherein the third sequence comprises a 256-bit sequence {-A, -A, -A, -A, A, -A, -A, A, -A, A, A, -A, -A, A, A, A, A, A, A, -A, -A, -A, A, A, -A, A, A, A, A, -A, A, -A, A, -A}.

17. (Original) The system of claim 16 wherein the circuitry for providing the secondary synchronization code comprises:

circuitry for performing an exclusive OR operation between the second sequence and the third sequence; and

circuitry for providing the secondary synchronization code in response to the exclusive OR operation.

18. (Currently amended) The system of claim 17:

wherein the second sequence comprises a plurality of code words; and

wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

19. (Original) The system of claim 18:

wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences;

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise seventeen Hadamard sequences selected as every eighth sequence in the defined order.

20. (Original) The system of claim 1:

wherein the primary synchronization code consists of 8-bit values A and B and complements of the values A and B;

wherein the value A comprises a sequence A = { 1, 1, 1, 1, 1, 1, -1, -1 };

wherein the value B comprises a sequence B = { 1, -1, 1, -1, 1, -1, -1, 1 };

wherein a value C is defined as a sequence C = { A, -B };

wherein the third sequence comprises a 256-bit sequence { C, C, C, -C, C, C, -C, -C, C, -C, C, -C, -C, -C, -C, -C }.

21. (Original) The system of claim 20 wherein the circuitry for providing the secondary synchronization code comprises:

circuitry for performing an exclusive OR operation between the second sequence and the third sequence; and

circuitry for providing the secondary synchronization code in response to the exclusive OR operation.

22. (Original) The system of claim 21:

wherein the second sequence comprises a plurality of code words; and

wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

23. (Original) The system of claim 22:

wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences;

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise sixteen Hadamard sequences selected as every sixteenth sequence in the defined order.

24. (Original) The system of claim 1 wherein the transmitter comprises a CDMA transmitter.

25. (Original) The system of claim 1 wherein the circuitry for providing the secondary synchronization code comprises storage circuitry for storing the secondary synchronization code.

26. (Original) The system of claim 25 wherein the secondary synchronization code stored by the storage circuitry is derived from an exclusive OR operation between the second sequence and the third sequence.

27. (Original) A method of forming a primary synchronization code and a secondary synchronization code for communication in a plurality of frames in a wireless communication system, comprising the steps of:

providing the primary synchronization code in response to a first sequence; and

providing the secondary synchronization code in response to a second sequence and a third sequence; and

wherein the second sequence is selected from a plurality of sequences, wherein each of the plurality of sequences is orthogonal with respect to all other sequences in the plurality of sequences; and

wherein the third sequence comprises a subset of bits from the first sequence.

28. (Original) The method of claim 27 wherein the first sequence comprises a hierarchical sequence.

29. (Original) The method of claim 27 wherein the first sequence comprises a Golay sequence.

30. (Original) The method of claim 27:

wherein the second sequence comprises a plurality of code words; and

wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

31. (Original) The method of claim 30 wherein the second sequence consists of fifteen of the code words.

32. (Original) The method of claim 31 wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences.

33. (Original) The method of claim 32:

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise sixteen Hadamard sequences selected as every sixteenth sequence in the defined order.

34. (Original) The method of claim 30 wherein the second sequence consists of sixteen of the code words.

35. (Original) The method of claim 34:

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise seventeen Hadamard sequences selected as every eighth sequence in the defined order.

36. (Original) The method of claim 27 wherein the step of providing the secondary synchronization code comprises:

performing an exclusive OR operation between the second sequence and the third sequence; and

providing the secondary synchronization code in response to the exclusive OR operation.

37. (Original) The method of claim 27:

wherein the primary synchronization code comprises 8-bit values A and B and complements of the values A and B;

wherein the value A comprises a sequence A = { 1, 1, 1, 1, 1, 1, -1, -1 };

wherein the value B comprises a sequence B = { 1, -1, 1, -1, 1, -1, -1, 1 }; and

wherein the primary synchronization code comprises a 256-bit sequence {A, B, A, B, A, B, -A, -B, -A, -B, A, B, -A, -B, -A, -B, A, B, A, B, A, B, -A, -B, A, B, -A, -B, A, B, A, B}.

38. (Original) The method of claim 37:

wherein the second sequence comprises 256 bits; and

wherein the third sequence comprises 32 repeated instances of the value A.

39. (Original) The method of claim 38 wherein the step of providing the secondary synchronization code comprises:

performing an exclusive OR operation between the second sequence and the third sequence; and

providing the secondary synchronization code in response to the exclusive OR operation.

40. (Original) The method of claim 39:

wherein the second sequence comprises a plurality of code words; and

wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

41. (Original) The method of claim 37:

wherein the second sequence comprises 256 bits;

wherein a complement of the value A is represented as –A; and

wherein the third sequence comprises a 256-bit sequence {-A, -A, -A, -A, A, -A, -A, A, -A, A, A, -A, -A, A, A, A, A, A, -A, -A, -A, A, A, -A, A, A, A, -A, A, -A, A, -A}.

42. (Original) The method of claim 41 wherein the step of providing the secondary synchronization code comprises:

performing an exclusive OR operation between the second sequence and the third sequence; and

providing the secondary synchronization code in response to the exclusive OR operation..

43. (Original) The method of claim 42:

wherein the second sequence comprises a plurality of code words; and

wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

44. (Original) The method of claim 43:

wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences;

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise seventeen Hadamard sequences selected as every eighth sequence in the defined order.

45. (Original) The method of claim 27:

wherein the primary synchronization code consists of 8-bit values A and B and complements of the values A and B;

wherein the value A comprises a sequence A = { 1, 1, 1, 1, 1, 1, -1, -1 }; wherein the value B comprises a sequence B = { 1, -1, 1, -1, 1, -1, -1, 1 };

wherein a value C is defined as a sequence C = { A, -B };

wherein the third sequence comprises a 256-bit sequence { C, C, C, -C, C, C, -C, -C, C, -C, C, -C, -C, -C, -C, -C }.

46. (Original) The method of claim 45 wherein the step of providing the secondary synchronization code comprises:

performing an exclusive OR operation between the second sequence and the third sequence; and

providing the secondary synchronization code in response to the exclusive OR operation.

47. (Original) The method of claim 46:

wherein the second sequence comprises a plurality of code words; and

wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

48. (Original) The method of claim 47:

wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences;

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise sixteen Hadamard sequences selected as every sixteenth sequence in the defined order.

49. (Original) The method of claim 27 wherein the step of providing the secondary synchronization code comprises providing the secondary synchronization code from a storage circuit.

50. (Previously added) A method of encoding a synchronization code, comprising the steps of:

producing a primary synchronization code comprising a first code sequence;

producing a secondary synchronization code comprising a second code sequence combined with a third code sequence, wherein the second code sequence is from a plurality of sequences, wherein each of the plurality of sequences is orthogonal with respect to all other sequences in the plurality of sequences, and wherein the third code sequence comprises a subset of bits of the first code sequence.

51. (Previously added) The method of claim 50 wherein the second code sequence comprises 256 bits, and wherein the third code sequence comprises 32 repeated instances of the a subset of bits from the first code sequence.

52. (Previously added) The method of claim 51 wherein the step of producing the secondary synchronization code comprises performing an exclusive OR operation of the second code sequence with the third code sequence.

53. (Previously added) The method of claim 52 wherein the second code sequence comprises a plurality of code words, and wherein each code word of the plurality of code words is selected from a plurality of Hadamard sequences.

54. (Previously added) The method of claim 50 wherein each of the second and third code sequences comprise 256 bits, and wherein the subset of bits from the first code sequence comprises a fourth code sequence of bits and a complement of the fourth code sequence of bits.

55. (Previously added) The method of claim 54 wherein the step of producing the secondary synchronization code comprises performing an exclusive OR operation of the second code sequence with the third code sequence.

56. (Previously added) The method of claim 55 wherein the second code sequence comprises a plurality of code words, and wherein each code word of the plurality of code words is selected from a plurality of Hadamard sequences.

57. (Previously added) The method of claim 56 wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences, wherein the 256 Walsh sequences have a defined order, and wherein the plurality of Hadamard sequences comprise seventeen Hadamard sequences selected as every eighth sequence in the defined order.

58. (Previously added) A method of decoding a synchronization code, comprising the steps of:

identifying a primary synchronization code comprising a first code sequence;

identifying a secondary synchronization code comprising a second code sequence combined with a third code sequence, wherein the second code sequence is from a plurality of sequences, wherein each of the plurality of sequences is orthogonal with respect to all other sequences in the plurality of sequences, and wherein the third code sequence comprises a subset of bits of the first code sequence.

59. (Previously added) The method of claim 58 wherein the second code sequence comprises 256 bits, and wherein the third code sequence comprises 32 repeated instances of the a subset of bits from the first code sequence.

60. (Previously added) The method of claim 59 wherein the second code sequence comprises a plurality of code words, and wherein each code word of the plurality of code words is selected from a plurality of Hadamard sequences.

61. (Previously added) The method of claim 58 wherein each of the second and third code sequences comprise 256 bits, and wherein the subset of bits from the first code sequence comprises a fourth code sequence of bits and a complement of the fourth code sequence of bits.

62. (Previously added) The method of claim 61 wherein the second code sequence comprises a plurality of code words, and wherein each code word of the plurality of code words is selected from a plurality of Hadamard sequences.

63. (Previously added) The method of claim 62 wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences, wherein the 256 Walsh sequences have a defined order, and wherein the plurality of Hadamard sequences comprise seventeen Hadamard sequences selected as every eighth sequence in the defined order.

64. (Previously added) A method of encoding a synchronization code, comprising the steps of:

producing a primary synchronization code comprising a first code sequence;

producing a secondary synchronization code comprising a second code sequence combined with a third code sequence, wherein the second code sequence is from a plurality of sequences, wherein each of the plurality of sequences is orthogonal with respect to all other sequences in the plurality of sequences, and wherein the third code sequence includes a plurality of subsets of

bits, each subset including a fourth sequence of bits from the first code sequence and a complement of a fifth sequence of bits from the first code sequence.

65. (Previously added) The method of claim 64 wherein the step of producing the secondary synchronization code comprises performing an exclusive OR operation of the second code sequence with the third code sequence.

66. (Previously added) The method of claim 65 wherein the second code sequence comprises a plurality of code words, and wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

67. (Previously added) The method of claim 66 wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences, wherein the 256 Walsh sequences have a defined order, and wherein the plurality of Hadamard sequences comprise sixteen Hadamard sequences selected as every sixteenth sequence in the defined order.

68. (Previously added) The method of claim 67:

wherein the primary synchronization code consists of 8-bit values A and B and complements of the values A and B;

wherein the value A comprises a sequence A = { 1, 1, 1, 1, 1, 1, -1, -1 };

wherein the value B comprises a sequence B = { 1, -1, 1, -1, 1, -1, -1, 1 };

wherein a value C is defined as a sequence C = { A, -B };

wherein the third sequence comprises a 256-bit sequence { C, C, C, -C, C, C, -C, -C, C, -C, C, -C, -C, -C, -C, -C }.

69. (Previously added) A method of decoding a synchronization code, comprising the steps of:

identifying a primary synchronization code comprising a first code sequence;

identifying a secondary synchronization code comprising a second code sequence combined with a third code sequence, wherein the second code sequence is from a plurality of sequences,

wherein each of the plurality of sequences is orthogonal with respect to all other sequences in the plurality of sequences, and wherein the third code sequence includes a plurality of subsets of bits, each subset including a fourth sequence of bits from the first code sequence and a complement of a fifth sequence of bits from the first code sequence.

70. (Previously added) The method of claim 69 wherein the second code sequence comprises a plurality of code words, and wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

71. (Previously added) The method of claim 70 wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences, wherein the 256 Walsh sequences have a defined order, and wherein the plurality of Hadamard sequences comprise sixteen Hadamard sequences selected as every sixteenth sequence in the defined order.

72. (Previously added) The method of claim 71:

wherein the primary synchronization code consists of 8-bit values A and B and complements of the values A and B;

wherein the value A comprises a sequence A = { 1, 1, 1, 1, 1, 1, -1, -1 };

wherein the value B comprises a sequence B = { 1, -1, 1, -1, 1, -1, -1, 1 };

wherein a value C is defined as a sequence C = { A, -B };

wherein the third sequence comprises a 256-bit sequence { C, C, C, -C, C, C, -C, -C, C, -C, C, -C, -C, -C, -C, -C }.